REMARKS

This application has been reviewed in light of the Office Action dated March 29, 2006, made final by the Examiner. Claims 1-16 are pending in the application. By the present amendment, claims 1 and 9 have been amended. Claims 32-35 have been canceled without prejudice. No new matter has been added. The Examiner's reconsideration of the rejection in view of the amendment and the following remarks is respectfully requested.

By the Office Action, claims 1-3, 6, 9-11 and 14 stand rejected under 35 U.S.C. 102(b) as being anticipated by JEDEC Publication JEP139 (hereinafter JEDEC).

JEDEC is directed to a test procedure which attempts to characterize stress-induced voids (SIPs) in test devices. The JEDEC procedure includes constant temperature baking to age samples, and the samples will not be sold are distributed to consumers. Nowhere in JEDEC are the steps of building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure, building the test structure including at least one of building a via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers and building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure, and thermal cycling the test structure for evaluating thermal cycle performance provided by the manufacturing process, disclosed or suggested.

Claim 1 now recites , *inter alia*, building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure, building the test structure including at least one of building a

via chain through layers of the semiconductor chip structure such that a plurality of widths of vias are used to adjust strain in different layers and building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure and thermal cycling the test structure for evaluating thermal cycle performance provided by the manufacturing process.

JEDEC fails to disclose or suggest at least these features. Claim 1 was amended to further clarify these distinctions. Claim 1 includes the subject matter of claims 32 and 33 and the phrase for evaluating thermal cycle performance provided by the manufacturing process. Claim 9 has also been amended in a similar manner as claim 1. Since JEDEC fails to disclose or suggest the previously described aspects of the present invention, claims 1 and 9 are believed to be in condition for allowance for at least the reasons stated. Claims 2-8 and 10-16 are also believed to be in condition for allowance due at least to their dependencies from claim 1 and 9, respectively. Reconsideration is earnestly solicited.

By the Office Action, claims 4-5, 12-13, 32 and 34 stand rejected under 35 U.S.C. 103(a) as being unpatentable over JEDEC in view of Suzuki et al. (PTO-892, pg 1,. NPL Reference V, hereinafter Suzuki), claims 7-8, 15-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over JEDEC in view of Huston et al. . (PTO-892, pg 1, NPL Reference W, hereinafter Huston), and claims 33 and 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over JEDEC in view of Yao et al. (U.S. Patent No. 6,864,701, hereinafter Yao).

Suzuki, Huston, and/or Yao fail to cure the deficiencies of JEDEC. Therefore, all pending claims are believed to be in condition for allowance over the cited art for at least the stated reasons. Reconsideration is earnestly solicited.

The Applicant notes with appreciation the telephonic interview granted by the Examiner, and the follow up communications. The Applicant appreciated the technical discussion and the Examiner's patience. The present amendments are believed not to raise any new issues, and the present case is believed to be in condition for allowance.

In view of the foregoing amendments and remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

It is believed that no additional fees or charges are currently due. However, in the event that any additional fees or charges are required at this time in connection with the application, they may be charged to applicant's IBM Deposit Account No. 50-0510.

Respectfully submitted,

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